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Electronic Version v1.1

Stylesheet Version v1.1.0

Title of Invention	Integrated Redundancy Architecture and Method for Providing Redundancy Allocation to an Embedded Memory System	
Application Number :		
Date :		
First Named Applicant:	Wayne F. Ellis	
Confirmation Number:		
Attorney Docket Number:	BUR920030151US1	
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Submitted By:		Elec. Sign.
Robert A. Walsh Esq. Registered Number: 26,516		Robert A. Walsh /s Attorney

Documents being submitted:	Files
us-fee-sheet	BUR920030151US1-usfees.xml us-fee-sheet.xsl us-fee-sheet.dtd
us-ids	BUR920030151US1-usidst.xml us-ids.dtd us-ids.xsl
us-assignment	BUR920030151US1-usassn.xml us-assignment.xsl us-assignment.dtd BUR920030151US1Assign1.tif BUR920030151US1Assign2.tif
us-request	BUR920030151US1-usrequ.xml us-request.dtd us-request.xsl
us-declaration application-body	BUR920030151US1Dec4.tif BUR920030151US1Spec-trans.xml us-application-body.xsl application-body.dtd wipo.ent mathml2.dtd mathml2-qname-1.mod isoamsa.ent isoamsb.ent isoamsc.ent isoamsn.ent isoamso.ent isoamsr.ent isogr3.ent isomfrk.ent isomopf.ent isomscr.ent isotech.ent isobox.ent isocyr1.ent isocyr2.ent isodia.ent isolat1.ent isolat2.ent isonum.ent isopub.ent mmlextra.ent mmlalias.ent soextblx.dtd BUR920030151US1drawing1.tif BUR920030151US1drawing2.tif
us-declaration	BUR920030151US1Dec1.tif
us-declaration	BUR920030151US1Dec2.tif
us-declaration	BUR920030151US1Dec3.tif
Comments	

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